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DRAFT PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	OCuLink Memory Map Change
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AFFECTED DOCUMENT:	OCuLink 1.0
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Part I

1. Summary of the Functional Changes

This is a modification of the cable assembly memory map defined in OCuLink 1.0, Appendix A. The addresses for the data bytes contained within the external cable assembly's memory will be reorganized.

In addition, some data in these fields are modified.

2. Benefits as a Result of the Changes

This aligns the OCuLink specification with the External Cable Specification for a common firmware development effort of cabled PCIe interfaces. The External Cable Specification 3.0 is aligned with the SFF-8636 specification that defines these memory maps and cannot be changed to match the released OCuLink specification.

The OCuLink specification was locked before the External Cable Specfication was aligned with the SFF working group.

3. Assessment of the Impact

Existing external OCuLink cable assemblies and ports must be modified to accept the new memory map organization.

4. Analysis of the Hardware Implications

The data contained in the memory within the external OCuLink cable assembly is changed from the current specification.

5. Analysis of the Software Implications

System management firmware must be modified to adjust to the new memory map.

6. Analysis of the C&I Test Implications

None, C&I does not currently exist.

Part II

Detailed Description of the change

Change Sections A.1 and A.2 as follows:

A.1. Lower Page Memory Map

The lower 128 bytes of page 00h are used to access a variety of cable information data. In addition, a mechanism to select upper memory map pages is provided. This portion of the address space is always directly addressable and, thus, is chosen for monitoring and control functions, which may need to be repeatedly accessed.

Table A-1. Bytes 0 to 127 (Lower Memory Fields)

Byte	Description	Value	Type	Notes
0	Identifier	18h	Read Only	Identifier for PCI Express OCuLink x4. In the 1.0 specification, this field contained 0Eh. If this value is read by firmware, then the memory map structure from the 1.0 specification must be used.
1- to 2	Status – Flat or paged		Read Only	See Table A-2
3- to 107	RsvpP			
108- to 109	Propagation Delay		Read Only	One-way propagation delay in nanoseconds
110	RsvdP			
111	PCIe Capabilities 1		Read Only	
112	PCIe Capabilities 2		Read Only	
113- to 118	RsvdP			
119- to 122	Password Change		Write-Only	See Section A.1.6
123- to 126	Password Entry		Write-Only	See Section A.1.6
127	Page Select Byte		Read/Write	For future expansion

Formatted Table

A.1.1. Identifier

Insert the same identifier value 18h into Byte 0 in the lower page (see Table A-1) and Byte 128 in the upper page 00h (see Table A-5, Byte 128).

A.1.2. Status

The Status indicator is used to indicate whether flat or paged memory is implemented and is defined in Table A-2.

Table A-2. Status Indicators

Address	Bit	Name	Description
1	All	RsvdZ	
2	0 to 1	RsvdZ	
	2	Flat_mem	Upper memory flat or paged. Flat memory: 0 = paging, 1 = page 00h only
	3 to 7	RsvdZ	

A.1.3. Propagation Delay

This is a 16 bit field to provide the one-way propagation delay through the cable assembly, pin-to-pin, in nanoseconds with fractional values rounded up. Byte 108 bit 7 is the most significant bit and Byte 109 bit 0 is the least significant bit. This information can be useful to the system to derive latency and timing information.

A.1.4. Cabled PCIe Capabilities 1

The Cabled PCIe Capabilities 1 register specifies capabilities supported by the cable assembly. The bit definitions and values are specified in Table A-3.

Table A-3. PCIe Capabilities 1 Bits (Address 111)

Bit	Description
3:7	RsvdP
2	Set if 8.0 GT/s capable, else Cleared
1	Set if 5.0 GT/s capable, else Cleared
0	Must be Set indicating 2.5 G T/s capable

The External Cabling specification defines bits 6:7. These functions are not applicable to this specification and are defined as RsvdP.

A.1.5. Cabled PCIe Capabilities 2

The Cabled PCIe Capabilities 2 register specifies capabilities supported by the cable assembly. The bit definitions and values are specified in Table A-4.

Table A-4. PCIe Capabilities 2 Bits (Address 112)

Bit	Description
Bits 7:3	RsvdP
Bits 2:0	Cable Assembly Width
	000b – x1
	001b – x2
	010b – x4
	011b – x8
	100b – x12
	101b – x16
	All other value Reserved

A.1.6. Password Change and Entry

Bytes 119~~123~~ to 126 are reserved for ~~an~~ the optional password entry function.

The p~~P~~assword entry bytes are retained until power down, reset, or rewritten by the ~~Host System~~fixed-side. These bytes are write-only.

~~Additionally, c~~Cable vendors are permitted to use this function to implement write protection of Serial ID and other read only information. Password access must not be required to access Free-side device data in either the lower memory page 00h or upper page 00h. Note that multiple manufacturer passwords are permitted to be defined to allow selective access to read or write to various sections of memory, as allowed above.

~~Host system~~ Fixed-side sub-system manufacturer and cable manufacturer passwords must be distinguished by the high order bit (bit 7, byte 123). All ~~Host system~~Fixed-side sub-system manufacturer passwords must fall in the range of 0000 0000h to 7FFF FFFFh, and all cable manufacturer passwords in the range of 8000 0000h to FFFF FFFFh. ~~System~~ Fixed-side sub-system manufacturer passwords must be initially set to 0000 1011h in new cables.

Passwords are permitted to be changed by writing a new password in Bytes 119 to 122 while the correct current password has been entered in 123 to 126, with the high order bit being ignored and forced to a value of 0b in the new password. The password entry field shall be set to 0000 0000h on power up and reset.

A.1.7. Page Select

Byte 127 is used to select the upper page. A value of 00h indicates upper memory page 00h is available to be mapped to locations 128 to 255. All other values are Reserved for future use.

A.2. Upper Page Memory Map

The upper page 00h contains the serial identifiers and is used for read-only identification information. The serial identifier is divided into the base level identifier, extended identifier fields, and vendor-specific data fields. The format of the Serial ID Memory Map is shown in Table A-5.

Table A-5. Upper Page 00h

Byte	Description	Value	Type	Notes
128	Identifier	18h	Read Only	See Notes for Byte 0 located in Table A-1
129	Extended Identifier		Read Only	See Table A-4
130	RsvdP			
131	Peripheral Power supported	Bit 0: two Lanes supported 0 = no 1 = yes Bits 7: 1 - RsvdP	Read Only	
132- to 146	RsvdP			
147	Cable Technology		Read Only	See Table A-5 and A-6
148 - to 163	Vendor Name	ASCII string (16 char)	Read Only	
164	RsvdP			
165- to 166	PCI-SIG Vendor ID	2 bytes	Read Only	
167	RsvdP			
168- to 183	Vendor Part Number	ASCII string (16 char)	Read Only	
184- to 185	Vendor Revision	Hex number (2 bytes)	Read Only	
186- to 189	Copper Cable Attenuation		Read Only	Copper cable attenuation, in dB, at: 1.25 GHz (Adr 186), 2.5 GHz (Adr 187), 4.0 GHz (Adr 188), and 8.0 GHz (Adr 189); values of all zeroes must be used for an active cable
190	Max. case temp			Maximum case temperature in degrees Celsius (if unspecified, 70 °C is assumed)
191	Checksum Base	Low order 8 bits of the sum of the contents of bytes 128- to 190		Checksum of Base ID fields (128- to 190)

Byte	Description	Value	Type	Notes
192- to 195	RsvdP			
196- to 211	Vendor Serial Number	ASCII string (16 Char)	Read Only	Serial number provided by vendor
212- to 217	Vendor Date Code	ASCII string (yymmdd)	Read Only	Vendor date code
218- to 219	Vendor Lot Code		Read Only	Vendor lot code (is permitted to be blank)
220- to 222	RsvdP			
223	Checksum Extended	Low order 8 bits of the sum of the contents of bytes 192- to 222		Checksum of Extended ID fields (192- to 222)
224- to 255	Vendor Specific Data		Read Only	Vendor-specific data